Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
100 level 2nd Semester Examination – Dec./Jan. 2016/17
CST161-3 Microcomputer Architecture and Logic Design

Uva Wellassa University

**Instructions to candidates**
**Duration:** Two (02) hours
**Number of questions:** Four (04)
**Answer all questions**
**Mark allocation:** 100

1.

a. Define positive logic system and negative logic system? (4 mark)

b. Simplify the Boolean expression **xy + x(wz + wz')** to a minimum number of literals. (2 mark)

c. Draw logic diagrams for the original and simplified expressions in **part b**. (4 mark)

d. Express the Boolean function **F = xy + x'z** as a product of sums. (4 mark)

e. Convert the function **F(A,B,C) = ∑(1,4,5,6,7)** into the form of **Maxterms** by taking the complement of the original function. (5 mark)

f. Simplify the Boolean function **F(A,B,C,D) = ∑(0,2,4,5,6,7,8,10,13,15)** using a Karnaugh map. (6 mark)

2.

a. Explain why the carry propagation time is an important attribute of the adder. (5 mark)

b. Implement a full adder with two (02) **4x1 multiplexers**. (5 mark)

c. Implement a full adder with a **3x8 decoder**. (5 mark)

d. Design a combinational circuit that converts the **8,4,-2,-1** code to **Gray code**. A truth table, Boolean equations and a logic diagram should be included. (10 mark)





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3.

a. What is a sequential circuit? (2 mark)

b. Draw a block diagram of a D flip-flop constructed using D latches with an enable pin and explain the operation of it. (4 mark)

c. Analyze the circuit given in Figure 1 and draw the state diagram (Hint: JK flip-flop characteristic table is given in Table 1). (7 mark)

Table 1: JK Flip-Flop Characteristic Table

| JK Flip-Flop | | | |
|---|---|---|---|
| **J** | **K** | **Q(t+1)** | **Note** |
| 0 | 0 | Q(t) | No change |
| 0 | 1 | 0 | Reset |
| 1 | 0 | 1 | Set |
| 1 | 1 | Q'(t) | Complement |

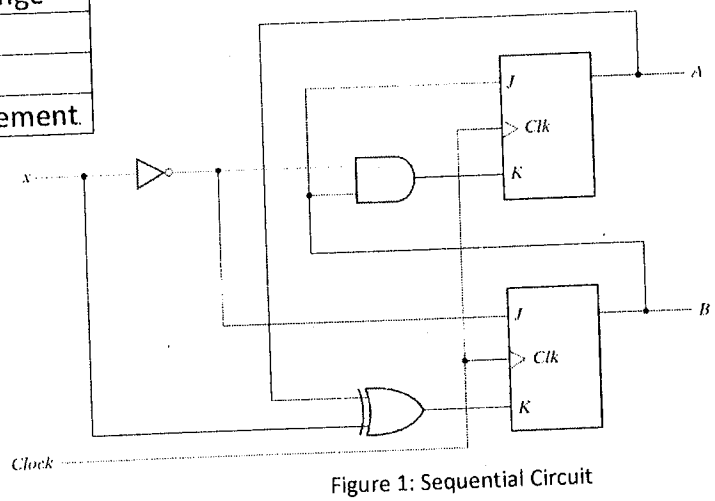


Figure 1: Sequential Circuit

d. Design a three-bit binary counter using T flip-flops by following the steps given below.

i. Draw the state diagram
ii. Draw the state table
iii. Derive T flip-flop input equations
iv. Draw the logic diagram

(12 mark)

4.

a. Explain the difference between **Mealy** model and **Moore** model. (4 mark)

b. Differentiate a register and a counter. (4 mark)

c. Explain the main difference of ripple counter and synchronous counter. (4 mark)

d. Draw the logic diagram of a **four-bit** shift register using **D flip-flops**. (4 mark)

e. Design a **four-bit** serial adder using shift registers and other required components. (9 mark)