Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
300 level 1st Semester Examination – Sept. / Oct. 2015
CST 331-2 Computer System Architecture

Uva Wellassa University

Instructions to candidates
Duration: two (02) hours
Number of questions: 5 Essay questions
Answers **(04) four** questions only
Mark allocation: 100 (All questions carry equal mark)

01.

a. Briefly describe, what is computer architecture?

(5 mark)

b. Briefly describe **three(03)** factors that used to measure the performance of a computer.

(4 mark)

c. Two computers A and B take time to run a program 19s, 26s respectively. Explain the comparison of A and B with their performance.

(5 mark)

d. Define the term **Cycle Per Instruction (CPI)** in computer architecture.

(4 mark)

e. Suppose that a Java program runs on a 2GHz processor with one billion instructions. Also 50% of the instructions execute in 3 clock cycles, 30% execute in 4 clock cycles, and 20% execute in 5 clock cycles. Find the **Clock Period** for the above processor and derive the execution time (**CPU Time**) of the Java program.

(7 mark)

02.

a. Briefly describe what is meant by **Instruction Set Architecture (ISA)** using your own word.

(4 mark)

b. Compile the C statement given below into MIPS assembly where r5 is the base address of ***save*** and i,j,k are stored in r3,r4,r5 respectively.

```
while ( save(i) == k )
i = i+j
```

(6 mark)

c. Transfer the following instructions to machine code using I and R formats. (use appropriate sample values)

```
lw r0, 1200(r1)
add r0, r2, r0
sw r0, 1200(r1)
```

(5 mark)

6

d. Find the 8 bit binary representation of **-4** using 2's complement method and derive 16 bit binary representation of -4 using **sign extension**.

(5 mark)

e. Describe the operations used in MIPS assembly to set some bits to 1, leave others unchanged with the aid of an example.

(5 mark)

03.

a. Explain what is **overflow** in integer addition.

(3 mark)

b. Describe the design of a multiplier using **Adders** and **Basic Gates** and explain how it works.

(6 mark)

c. Give the MIPS instruction for **arithmetic division** and describe how its works.

(4 mark)

d. Explain **Std IEEE 754-98(single precision)** floating point representation with a simple example

(7 mark)

e. Explain the steps how two floating point numbers can be added in computer arithmetic and follow the prescribe steps to add 0.5, –0.4375 (do this using 4-digit binary)

(5 mark)

04.

Answer the following questions using the circuit diagram given below in Figure 1.

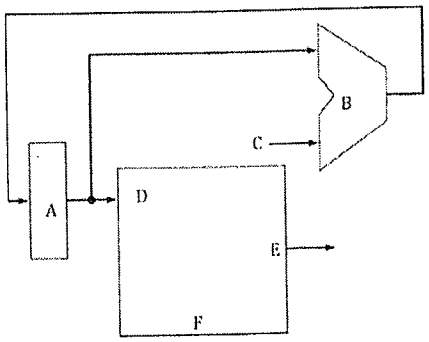

Figure 1

a. Name the components **A,B,F** and points **D,E**.

(5 mark)

b. Find the suitable value for **C** and clearly indicate your justification for the value.

(3 mark)

c. Briefly explain the functionality of **A** and find the size of the output line from B and E.

(4 mark)

d. Briefly explain how multiplexer can be used to improve the functionality of the circuit diagram given in Figure 1.

(4 mark)

e. Briefly explain the use of pipeline in processor and list all the stages of processor pipeline.

(4 mark)

f. Explain what is structural hazard and how to solve it.

(5 mark)

05.

a. Briefly describe what is **Temporal Locality** and give **three (03)** advantages of it.

(5 mark)

b. State the usage of cache memory in memory management.

(3 mark)

c. Explain the difference of **Direct mapping, 2-way set associative mapping, Fully associative mapping** in cache mapping.

(6 mark)

d. Derive the best cache mapping method given in (c) using 4 block cache memory with the block access sequence of 0, 8, 0, 6, 5, 8, and 6.

(4 mark)

e. Explain how **Least Recently Used (LRU)** cache replacement algorithm works with the aid of block references 0 ,1 ,2 ,3 , 0 ,1 ,4 ,0 ,1 ,2 ,3 ,4 ,1,0.

(7 mark)