Uva Wellassa University, Sri Lanka
End Semester Examination – February/March 2012
SCT 361-2 Digital and Analog Electronics & Repeat

Time: Two (02) Hours

Total **04** Questions
Answer **all** questions

1)

I. Describe the Ebers-Moll (EM) model of the npn transistor using suitable sketches.

(25 marks)

II. Prove the following

a) $$i_E = \left(\frac{I_S}{\alpha_F}\right)(e^{v_{BE}/V_T} - 1) - I_S(e^{v_{BC}/V_T} - 1)$$

b) $$i_C = I_S(e^{v_{BE}/V_T} - 1) - \left(\frac{I_S}{\alpha_R}\right)(e^{v_{BC}/V_T} - 1)$$

c) $$i_B = \left(\frac{I_S}{\beta_F}\right)(e^{v_{BE}/V_T} - 1) + \left(\frac{I_S}{\beta_R}\right)(e^{v_{BC}/V_T} - 1)$$

where $\beta_F = \frac{\alpha_F}{1-\alpha_F}$ and $\beta_R = \frac{\alpha_R}{1-\alpha_R}$

$$i_{DE} = I_{SE}(e^{v_{BE}/V_T} - 1)$$

$$i_{DC} = I_{SC}(e^{v_{BC}/V_T} - 1)$$

(75 marks)

2)

I. Explain how an OPAMP can be used as a comparator.

(10 marks)

II. Draw basic schematic diagrams of both inverting and non-inverting amplifiers.

(14 marks)

III. Derive expressions for closed loop gain (G) of both inverting and non-inverting amplifiers.

(20 marks)

IV. Identify the circuit given in Fig. 2.1.

a. Derive an equation for its output in terms of inputs and component values.

(22 marks)

b. Describe functionality and its' practical applications.

(14 marks)

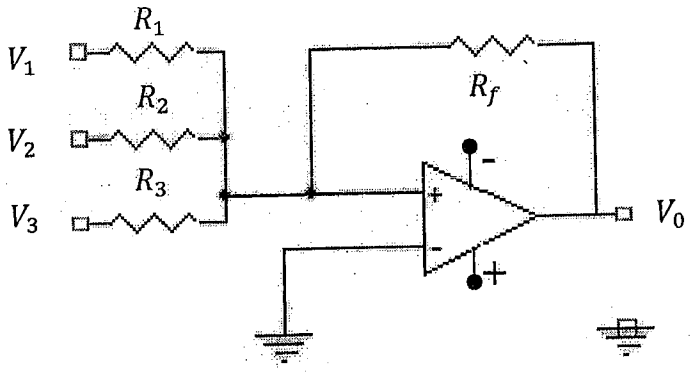

Fig. 2.1

V. Explain the basic integrator circuit using ideal OPAMPs.

(20 marks)

3)

I. Simplify the following expressions using Boolean Algebra:

a. X = (A + B + A.B) . (A + B) .A.B

b. Y = (A + B + A.B) .C

(30 marks)

II. F = A.B .C .D + A.C + B .C .D + B .C + A.C .D + A.B .C .D

Show that F can be simplified to F_1 using a **Karnaugh map**

F_1 = A.B + A.B + A.C + B .C .D

(20 marks)

III. Show how F_1 can be implemented using NAND gates and draw the circuit diagram. Assume that complemented input variables are available.

(25 marks)

IV. Draw the truth table for BCD to 7 Segment display and implement only one circuit to display "1" at the 7 segment display.

(25 marks)

4)

I. Show how two 2-input NOR gates can be connected together to implement an RS latch. Describe its operation and write down its truth table.

(50 marks)

II. A synchronous binary up-counter having the state sequence as follows is to be implemented using three D-type flip-flops.

1, 2, 3, 4, 5, 6, 1, 2, . . .

The flip-flop outputs are designated Q_2, Q_1 and Q_0, where Q_0 represents the least significant digit of the count.

Give simplified expressions for the required next-state logic.

(50 marks)