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Uva Wellassa University, Sri Lanka

Faculty of Science and Technology

Computer Science and Technology Degree Program

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CST 331-2 Computer Systems Architecture

Uva Wellassa University

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Instructions to Candidates

This paper will contains **Four Essay Questions.**

Answer **all** questions.

Q1.

a. Define the term Computer Architecture.

b. What is the main difference between the responsibilities of a hardware designer and a computer architect?

c. Briefly explain the **Stored Program Principal** in Von Neumann Architecture.

d. "The Modern Computer incorporates aspects of both Harvard Architecture and Von Neumann Architecture". Comment on the above statement with examples.

e. Briefly explain the **Fetch – Decode – Execution** cycle in stepwise.

Q2.

a. Briefly explain the pipelining technique in modern computers by using a suitable example.

b.

i. What is the reason of introducing the logical memory addresses in 8086 microprocessor architecture?

ii. During execution of a program, the SS contains 04500H, DS contains 05000H, CS contains 05500H and IP contains 0050H. Calculate the physical address for the next instruction to be executed in the program.

c. The following is a part of the data segment during the execution of a program in Intel 8086. Answer the following questions based on this data segment.

Offset	
5509H	2C
5508H	10
5507H	22
5506H	B3
5505H	37
5504H	A2
5503H	FF
5502H	25
5501H	6A
5500H	34

i. Using the Indirect memory addressing mode, increase the value stored at offset 5501H by 4.

ii. For each of the following, determine the value of each operand (in hexadecimal format) after execution of the instructions.

Assume that BX = 5505H

1. INC BX
2. MOV AX, WORD PTR[BX]
3. SUB BX,0002H
   MOV AX,10H
   ADD AX, WORD PTR[BX+3]

iii. Write **only the necessary instructions** to add the values from offsets 5502H to 5503H and store the result at the offset 5504H.

Hint - The resultant sum is a value greater than 255 and less than 65535.

iv. Assume that a five-element word array (named ARR) is defined at the offset 5505H. Using the Indexed memory addressing mode divide 2nd element of array by 4th element and stores the quotient part at the offset 5500H and remainder at the offset 5501H. Write **only necessary instructions** that should come under the code segment.

d. Briefly explain the use of having stack memory segment. What is the use of IRET instruction?

Q3.

a. Briefly explain the difference between static RAMs and dynamic RAMs.

b. A cache memory is referencing five memory blocks, A, B, C, D and E, in the following order:

A; B; D; C; A; E; B; C; B; D; A; E;

Assume that the cache memory can only store three memory blocks at a given time. Draw the content of the cache memory during each reference, if least recently used replacement algorithm is used.

b. What is the purpose of having a virtual memory in a computer system?

c. What is a Protocol in terms of I/O subsystem?

d. Compare and contrast Programmed I/O control method and Interrupt-Driven I/O control method.

Q4.

Implement the following C code in MIPS, assuming that the set_array is the first function called. Assume that the variables a, b and i corresponds to the registers $a0, $a1 and $a2 respectively. Base address of the array is related to the register $s0.

```
int i;
void set_array(int num){
        int array[10];
        while(i<10){
                array[i]=compare[num,i];
        }
}

int compare(int a, int b){
        if(a<b)
                return 1;
        else
                return 0;
}
```

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