Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
100 Level 2nd Semester Examination – Jan. / Feb. 2016
CST 151-3 Microcomputer Architecture and Logic Design

Instructions to candidates:
Duration: Two (02) hours
Number of questions: Four (04)
Answer all questions
Mark allocation: 100
Calculators are **allowed.**
This paper consist of two (02) parts: Part – A and Part – B.

Part – A

1.

a. State the **DeMorgan's theorem** for Boolean expressions.

(2 mark)

b. Simplify the following Boolean expressions to a minimum number of literals. Clearly state the intermediate steps and rules used.

i. $AB + A(B + C) + B(B + C)$
ii. $A + AB + A\overline{B}C$
iii. $A + (A + \overline{C})(A + B)$

(9 mark)

c. Simplify the following Boolean expressions, using **Karnaugh maps**.

i. $A\overline{B} + AB$
ii. $\overline{A} + A\overline{B} + AB\overline{C}$
iii. $\overline{A}BC + A\overline{B}C + AB\overline{C} + ABC$

(12 mark)

d. Construct a Boolean expression that simulates the functionality of **XOR addition**. The expression must be comprised of only basic operations such as AND, NOT and OR.

(2 mark)

2.

a. A machine has 4 fail-safe sensors. The machine should keep running unless any of the following conditions arise:

- If sensor 1 is activated.
- If sensor 2 and sensor 4 are activated together.
- If sensor 3 and sensor 4 are activated together.

i. Derive the truth table for the above scenario.

(4 mark)

ii. Simplify the boolean expression for the output using a Karnaugh map.

(6 mark)

ii. Construct a logic gate network to satisfy above requirements with basic logic gates.

(4 mark)

iii. Re-design the developed logic gate network with **NAND** gates only.

(4 mark)

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b.

i. Distinguish **combinational** and **sequential** logic circuits. (2 mark)

ii. What are the **two (02)** major types of sequential circuits? (2 mark)

c. Discuss the importance of the concept "**synchronization**" in context of coupling heterogenous devices. (3 mark)

3.

a.

i. What is meant by a **Latch**? (2 mark)

ii. Explain the difference between an **active-high** and **active-low** types of **SR (Set/Reset) latch**. (6 mark)

iii. Explain how the functionality of a typical **SR latch** can be extended by adding an "**enable**" input. (4 mark)

iv. What is the key difference between the **SR latch** and **D latch**? (2 mark)

b.

i. Compare and contrast the functionality of the **JK flip-flop** against **clocked D flip-flop**. (4 mark)

ii. List **three (03)** applications of **JK flip-flops** except as a frequency divider. (3 mark)

c. Explain how a **frequency divider** can be constructed from **J-K flip-flops** using appropriate circuit diagrams. (4 mark)

4.

a.

i. What is meant by a **ripple counter**? (2 mark)

ii. Implement a **three (03) bit** asynchronous ripple counter using **J-K flip-flops**. (4 mark)

iii. Discuss the requirement of **synchronous counters** in the context of **cumulative delay**. (3 mark)

b. Explain how a **BCD or decade counter** can be constructed from a **4 bit ripple counter**. (4 mark)

c.

i. Why we need **full-adder** while the **half-adder** is capable of performing bit wise addition? (2 mark)

ii. Construct a full-adder using **two (02) half adder** units. (4 mark)

iii. Explain how a **4 bit full-adder** can be converted in to a **substractor**. (4 mark)

d. Differentiate **Multiplexers** against **Demultiplexers**. (2 mark)