Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
100 level 2nd Semester Examination – Dec. - 2017/Jan. - 2018
CST161-3 Microcomputer Architecture and Logic Design

Uva Wellassa University

Instructions to candidates
Duration: Two (02) hours
Number of questions: Four (04)
Answer all questions
Mark allocation: 100

1.

a. Represent the decimal number 5,137 in Binary-Coded Decimal (BCD) and excess-3 code? (4 mark)

b. Simplify the Boolean expression **ABCD + A'BD + ABC'D** to two literals. (2 mark)

c. Draw two logic diagrams for the original and the simplified expressions in **part b**. (5 mark)

d. Construct a truth table for the function **F= x'z' + yz**. (4 mark)

e. Express the complement of the function **F(A,B,C,D) = ∑(3,5,9,11,15)** in sum-of-minterms form. (4 mark)

f. Simplify the Boolean function **F(w,x,y,z) = ∑(1,3,7,11,15)** which has the don't-care conditions **d(w,x,y,z) = ∑(0,2,5)** using a Karnaugh map. (6 mark)

2.

a. Explain the importance of carry propagation time of the adder. (5 mark)

b. List the truth table of an Octal-to-Binary Encoder. (5 mark)

c. Implement a full adder with a **3x8 decoder**. (5 mark)

d. Design a combinational circuit with three inputs x, y and z and three outputs A, B and C. When the binary input is 0, 1, 2, or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is three less than the input. A truth table, Simplified Boolean equations and a logic diagram should be included. (10 mark)

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3.

a. Differentiate Lathes vs. Flip-Flops. (2 mark)

b. Draw a block diagram of the SR latch with NAND gates and construct a functional table of the circuit. (4 mark)

c. Analyze the circuit given in Figure 1 and draw the state diagram (Hint: JK flip-flop characteristic table is given in Table 1). (7 mark)

Table 1: JK Flip-Flop Characteristic Table

JK Flip-Flop			
J	K	Q(t+1)	Note
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

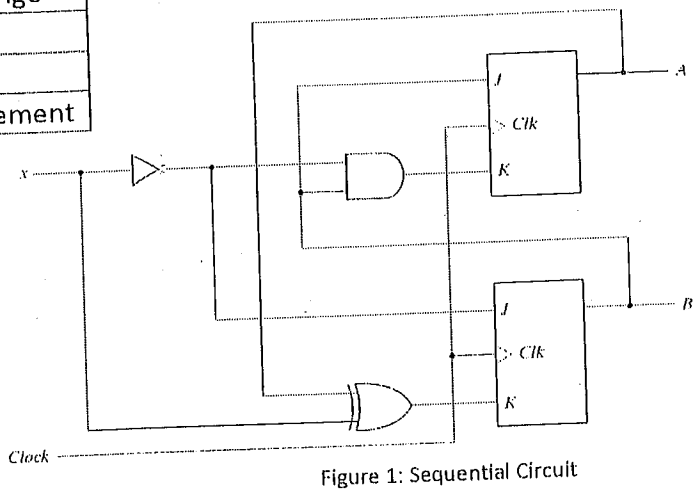

Figure 1: Sequential Circuit

d. Design a sequential circuit with two D flip-flops A and B and one input x. When x=0, the state of the circuit remains the same. When x=1, the circuit goes through the state transitions from 00 to 01, to 11, to 10, back to 00, and repeats. Use the following steps to design the circuit.

i. Draw the state diagram
ii. Draw the state table
iii. Derive D flip-flops input equations
iv. Draw the logic diagram

(12 mark)

4.

a. Explain the difference between **Mealy** model and **Moore** model. (4 mark)

b. Differentiate ripple counters vs. synchronous counters. (4 mark)

c. Draw a block diagram of the 4-bits ripple counter using T flip-flops. (5 mark)

d. Draw a logic diagram of a **four-bit** shift register using **D flip-flops**. (4 mark)

e. Design a **four-bit** serial adder using shift registers and other required components. (8 mark)