Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
300 level 1st Semester Examination – May/Jun. 2017
CST331-2 Computer Systems Architecture

Uva Wellassa University

Instructions to candidates
Duration: Two (02) hours
Number of questions: Four (04)
Answer all questions
Mark allocation: 100

1.

a. What are big-endian and little-endian fashions of Byte-addressable memories? (5 mark)

b. Illustrate R-type and J-type instruction formats of MIPS architecture. (5 mark)

c. Explain the five (05) addressing modes of MIPS architecture? (10 mark)

d. Explain the purposes of jump and link instruction (jal) and jump register instruction (jr). (5 mark)

2.

a. Explain the following MIPS code using comments for each line and write one sentence to explain the whole process of the given MIPS code.

```
        add $t0, $zero, $zero
loop:   beq $a1, $zero, finish
        add $t0, $t0, $a0
        sub $a1, $a1, 1
        j loop
finish: addi $t0, $t0, 100
        add $v0, $t0, $zero
```

(9 mark)

b. Depict the structures of Instruction Memory and Data Memory of MIPS processor. (8 mark)

c. Illustrate the single cycle processor for **sw** and **lw** instructions of the MIPS architecture with appropriate labels. (8 mark)

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3.

a. Explain the following five (05) stages of the pipelined processor.
   i. Fetch stage
   ii. Decode stage
   iii. Execute stage
   iv. Memory stage
   v. Write-back stage

(10 mark)

b. Differentiate single-cycle processor vs pipelined processor. (8 mark)

c. Describe the main two (02) categories of hazards in pipelined processors. (7 mark)

4.

a. Explain Hit Time and Miss Penalty according to memory systems. (5 mark)

b. Describe direct mapped cache, N-way set associative cache and fully associative cache. (9 mark)

c. Explain the three (03) main cache misses. (6 mark)

d. Compare write-trough and write-back policies of cache memory. (5 mark)