Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
End Semester Examination – August/September 2014

CST 231 – 2 Microelectronics

Number of questions: Four (04)
Answer all questions
Time allocation: Two (02) hours
Total mark: 100

1.

a. What is the purpose of a transducer? (3 mark)

b. A signal source has an open-circuit voltage of **10mV** and a short-circuit current of **10μA**. What is the source resistance? (3 mark)

c. What is a digital signal? (3 mark)

d. Consider a **4 bit** digital word $\mathbf{b_3b_2b_1b_0}$ in a format called unsigned-magnitude and it does not represent any negative values. This digital word represents an analog signal (v_A) which varies between 0V and 15V.

i. Give digital word corresponding to v_A=0V,1V,2V and 15V. (4 mark)

ii. What does happen to v_A if the value of b_0, b_1, b_2 and b_3 is changed from 0 to 1? (1.5x4=6 mark)

e. If v_A=5.2V, what is the digital code expected? What is an error percentage? (6 mark)

2.

a. Construct three input AND gate and OR gate using diodes (You can use your own notations for inputs and output).

(2x3=6 mark)

b. In the ideal-diode circuit shown in the Figure 1, v_i is **1KHz, 10V** peak sine wave. Sketch the resultant waveform at v_o. What are its positive and negative peak values? (5 mark)

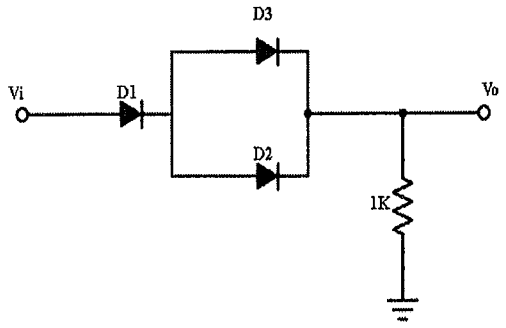


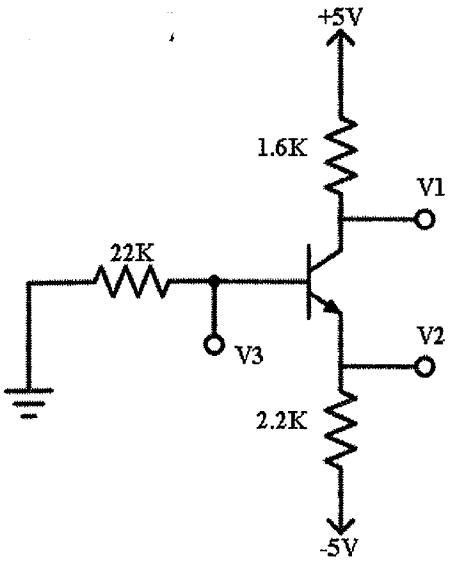
Figure 1. Ideal-diode circuit

c. List and explain all steps in IC fabrication. (14 mark)

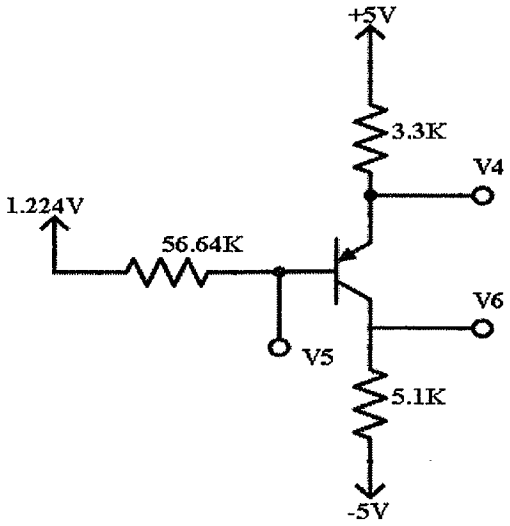
3.

a. Draw the simplified structure of **npn** bipolar junction transistor (indicate all junctions). Write all the modes of bipolar junction transistors and corresponding bias condition of each **pn** junctions. (9 mark)

b. Find the values for the labeled nodes voltage and branch current for Circuit 2 and Circuit 3. Write all necessary steps.
(Assume $\beta = 100$ and $|V_{BE}| = 0.7V$.) (8 x 2 =16 mark)



Circuit 1



Circuit 1

4.

a. Construct CMOS logic circuits for two inputs NOR gate and two inputs NAND gate. (8 mark)

b. Sketch a CMOS logic circuit that realizes the function $y=\overline{A(B+CD)}$. (8 mark)

c. Draw the graph of the voltage transfer characteristic of an inverter. (5 mark)

d. Draw the circuit diagram of the CMOS digital logic inverter. (4 mark)

07