Uva Wellassa University, Sri Lanka

End Semester Examination – September/October 2012

SCT 363-2 Advanced Electronics

Uva Wellassa University

Time: Two (02) hour

Total **04** questions

Answer **all** questions

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1.

a) Briefly explain the difference between an active filter and a passive filter.

b) Identify the circuit diagram in figure 01.

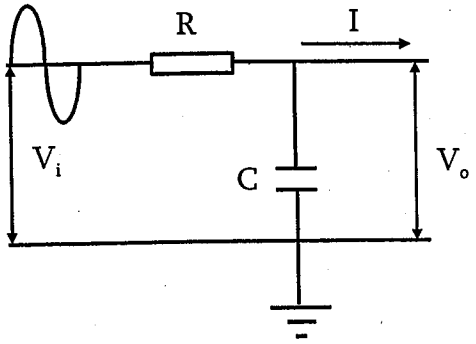

Fig. 01

c) Plot the graph of gain (V_o/ V_i), against frequency for above circuit.

d) Using response curves, relevant equations and circuit model explain

i. First order band-pass passive CR filter circuit.

ii. First order low pass OPAMP circuit.

e) For the following OPAMP circuit find the expression for V_o

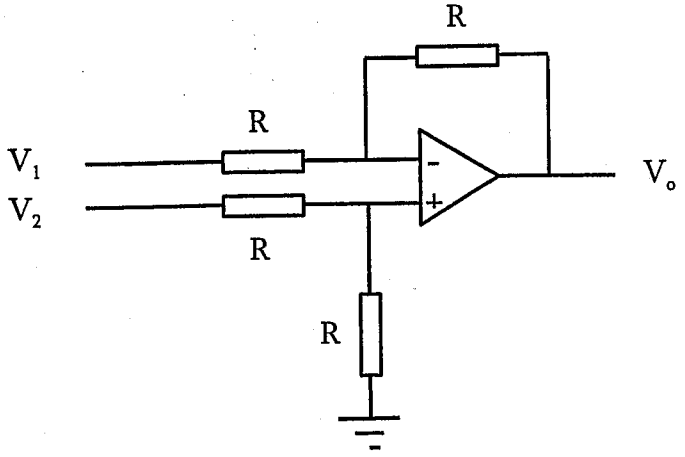

Fig. 02

(25 marks)

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2.

a) State the sampling theorem in signal transmission.

b) Briefly explain how information is lost during the process of analog conversion (ADC).

c) Compare the single slope ADC with dual slope ADC.

d) Draw the typical schematic diagram of a single slope ADC.

(25 marks)

3.

a) Draw a schematic representation for a single bit memory. Briefly explains the "Read" and "Write" operations using the above representation.

b) Write short notes for three (03)of the following topics

i. SRAM

ii. DRAM

iii. EPROM

iv. EEPROM

c) Draw the circuit diagram to show how you would construct a 2kB (2048*8 bit) memory using two 1kB (1024*8 bit) RAM.

(25 marks)

4.

a) Briefly explain the two types of address decoding methods.

b) What is parity checking in memory address decoding?

c) Suppose you are expected to design a microprocessor based system using an 8 bit microprocessor having 16 address lines and other necessary control lines. You are also provided with the following devices together with a switch to interface with the microprocessor.

Device	Size	Starting address
Flash memory	2kB (2048*8 bit)	0000H
EEPROM chip	2kB (2048*8 bit)	2000H

The switch should be interfaced using the memory mapped method. Its address is 7301H.

i. Draw the memory map of the system

ii. Draw a circuit diagram of the system showing all the address decoding circuits. (You may use additional gates if necessary)

(25 marks)