CMOS Analog Integrated Circuits for Cochlear Implant System

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Introduction

For centuries, people believed that it's a miracle to restore hearing to the complete disability of hearing (deaf). About forty years ago scientists first attempted to restore normal hearing to the deaf by electrical stimulation of the auditory nerve (Philipos, 1998). With the modern developments, the auditory sensations elicited by electrical stimulation give comfortable hearing for the deaf people. Final product of the latest research called "cochlear implant",which can be implanted in the inner ear and can restore partial hearing to profoundly deaf people.Patients withcochlear implants can now communicate without lip-reading or signing, and some can communicate even over the telephone.

This paper describes the design and simulation of a low power signal processor which can be used as analog signal processor of main Cochlear implant system using 0.13 μm CMOS technology. The signal processor circuit which is made up of band pass filter, envelop detector and dual slope convertor are based on newly design operational transconductance amplifier (OTA).The propose system has been designed using CMOS technology by means of Cadence CAD tool. The simulations were performed under normal condition using Hspice Simulator and Cscope graphical circuit simulator software for Linux.

Methodology

Figure 1(a) represents the operational overview of the multi channel cochlear implant system as a flow chart (Germanovix and Toumazou, 2000). In this research, for each channel we introduced the propose OTA and subsidiary units for the design. The OTA circuit as shown in figure 1(b) has a differential pair input, current source and adding cascode MOSFETs for reducing the output swing which consists eight PMOS and eight NMOS transistors.

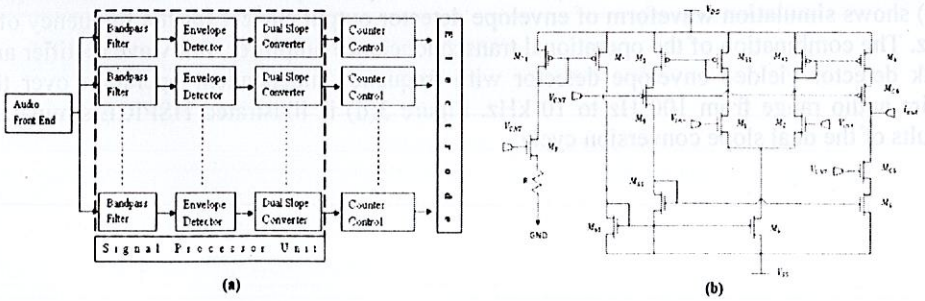

Figure 1: (a) Overview of the multi channel cochlear implant system (b) OTA circuit

The band pass filter shown in figure 2(a) is a first order transconductance capacitor filter and consists of interconnected lowpass and highpass filters and two stages of capacitive attenuation. The bandpass filter technology offers a number of advantages for signal processing circuit design. It operates at low voltage with large dynamic range. Here a capacitive attenuation technique is added for cancelling noise. Everyone's hearing loss is different and thus the signal processor needs to be tuned to the particular hearing frequency band. There is possibility to tune bandpass filter over a wide frequency range. The envelop detector shown in figure 2(b) consists three devices; full wave rectifier, transconductance amplifier and peak detector. Dual slope converter is localized between envelop detector and programmable counter in each channel of the signal processor. It is consists of an OTA, integrating capacitor, operational amplifier as comparator and control logic unit with counter as shown in figure 2(c).

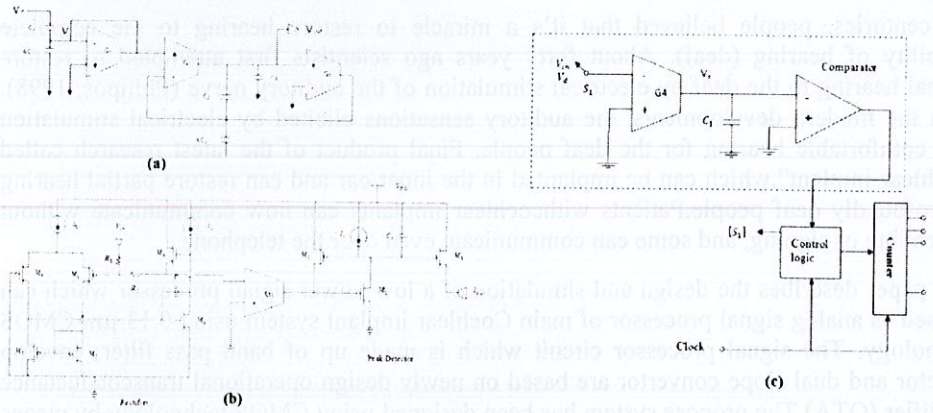

Figure 2: (a) Bandpass Filter with Capacitive Attenuation(b) Architecture of envelope detector (c) Dual slope analog to digital converter

Results

Figure 3(a) shows how the magnitude of the gain of the OTA varies over the frequency. The 3dB down frequency of the amplifier is approximately 100 kHz and the gain is approximately 60dB. Therefore OTA operates under low voltage which is the main advantage of this design. Figure 3(b) shows the frequency response of the bandpass filter apropos 5 kHz frequency band. The pole at 5 kHz drops the phase to 90° from -90°. Figure 3(c) shows simulation waveform of envelope detector output current for the frequency of 1 kHz. The combination of the operational transconductance amplifier, full wave rectifier and peak detector yielded envelope detector with frequency independent operation over the entire audio range from 100 Hz to 10 kHz. Figure 3(d) is illustrated HSPICE simulation results of the dual slope conversion cycle.

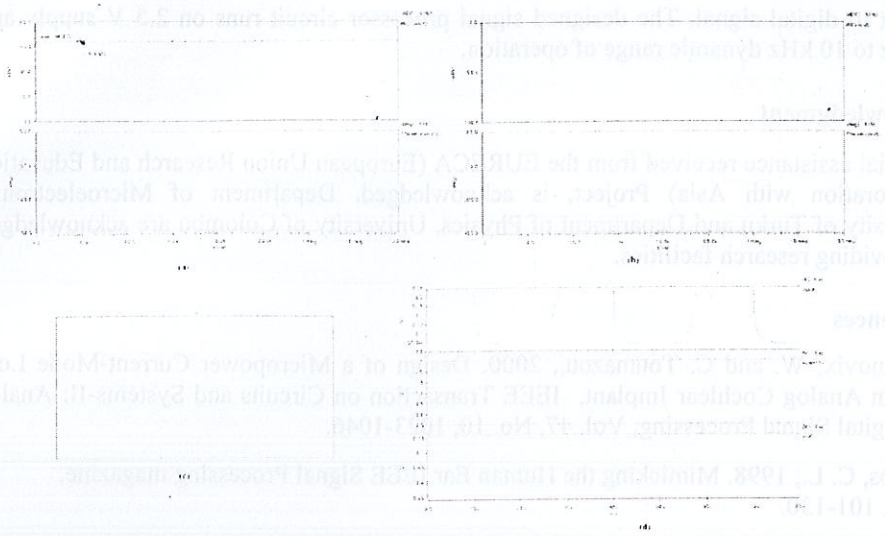

Figure 3: (a) Frequency response of the OTA (b) Frequency response of Bandpass Filter (c) Peak Detector output waveform (d) A comparator and dual slope output waveforms

Discussion and Conclusions

This paper explored the approach of low-voltage OTA design using the cascode technique and 0.13 micrometer CMOS technology. Adding cascode MOSFETs for the design was to reduce the output swing which was reported by the researches (Sarpeshkar*et al.*, 1998)

The design of such low voltage, high performance OTA circuit on 0.13 micrometer technology satisfies the required parameters for its implementation not only in power saving devices but also in biomedical portable devices like biomedical implantable sensors, disk read channel integrated circuits (ICs), video filters, ADSL front-ends, and RF ICs.

This signal processor should be useful in bionic implants for the deaf people as their hearing aids and also as low power speech recognition system. A number of signal processing algorithms including equalization, dynamic range compression and directional processing have already been implemented. Therefore it is suitable for audio front-end processing in telecom applications, speech recognition systems or hearing aids. Stereo mode is proving particularly useful for frequency domain directional processing.Table 1 shows the summarized technical final specification of the each design.

Table 1: Technical Specification Sheet

Name of circuit	Number of NMOS	Number of PMOS	Gain	Bandwidth	Supply voltage
OTA	8	8	60 dB	100 kHz	2.5 V
Bandpass filter	24	24	-	100 Hz-10 kHz	2.5 V
Envelop detector	10	15	-	-	2.5 V
Dual slope convertor	13	13	-	-	2.5 V

Finally,it can be concluded that, this design of signal processor can be used to CMOS Cochlear implant system as channels because output signals of bandpass filter arrays can be

convert to digital signal. The designed signal processor circuit runs on 2.5 V supply and 100 Hz to 10 kHz dynamic range of operation.

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