

Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
100 level 1st Semester Examination – Sept. / Oct. 2015
CST 131-2 Microcomputer Architecture and Logic Design



Instructions to candidates:

Duration: **Two (02) hours**

Number of questions: **Four (04)**

Mark allocation: **100**



1

- a.
- i. Express the binary number 10101.101 in decimal. (3 mark)
 - ii. Convert $(11.375)_{10}$ to binary. (5 mark)
- b.
- i. Given the two binary numbers $X = 01101_2$ and $Y = 01001_2$, perform the subtraction of $X - Y$ using 2's complement. (5 mark)
 - ii. **(r-1)'s complement** of any number system is given by the a general formula $\{(r^n)_{10} - 1\} - N$
where, r = Radix or base of the number system, n = Number of digits and N = Number.
Find **8's complement** of octal number $(465)_8$ using the general formula.
(Hint: In order to find 8's complement of $(465)_8$, first you have to find 7's complement of $(465)_8$). (5 mark)
- c. Express the **BCD (Binary Coded Decimal)** code for the number $(568)_{10}$. (5 mark)
- d. What is the **Gray Code** for nine (9)? (2 mark)

2.

- a.
- i. Design an equivalent circuit for Exclusive OR (XOR) gate with basic types of logic gates. (4 mark)
 - ii. Write the Boolean expression for the output for above (2.a.i.) developed circuit. (4 mark)
- b. Simplify the following Boolean expressions to a minimum number of literals. Clearly state the intermediate steps and the rules used.
- i. $C + (BC)'$
 - ii. $(AB)'(A' + B)(B' + B)$
 - iii. $(A + C)(AD + AD') + AC + C$ (9 mark)

c. Simplify the following Boolean functions, using **Karnaugh maps**.

i. $f(A,B,C) = A'B + BC' + BC + AB'C'$

ii. $f(X,Y,Z) = XYZ + XYZ' + XY'Z + XY'Z' + X'YZ + X'Y'Z + X'Y'Z'$ (where $X' = \text{not } X$)

(8 mark)

3.

a. Explain the difference between **combinational** and **sequential logic**.

(5 mark)

b. An airbag of a vehicle is activated once the following conditions meets:

- Engine must be running (Logic Level of sensor 'E' is High)
- The driver / passenger has buckled-up (fasten) the seat belt (Logic level of sensor 'B' is Low)
- Speed sensor 'S' has exceeded the threshold value. (Logic level High)
- Vibration sensors both 'V1' and 'V2' together or 'V3' alone is triggered. (Logic level High)

i. Construct the truth table for the above (3.b.) scenario.

(5 mark)

ii. Construct a logic gate network to satisfy (3.b.) requirements with basic logic gates.

(5 mark)

iii. Re-design the (3.b.i.) developed logic gate network with NAND and NOR gates only.

(5 mark)

iv. If the delay experienced in a NAND gate and NOR gate is 8 and 12 seconds respectively, what is the overall expected delay?

(5 mark)

4.

a.

i. What are the most common types of flip-flops?

(3 mark)

ii. Explain the functionality of each (4.a.i.) listed flip-flop.

(8 mark)

b. A decoder is a circuit that takes an n-digit binary number as the input and decodes it into 2^n data lines. For example, a decoder with 3 binary inputs ($n = 3$), would produce a 3-to-8 line decoder. ($2^3 = 8$ output data lines.) The simplest is the 1-to-2 binary decoder (Figure 1).

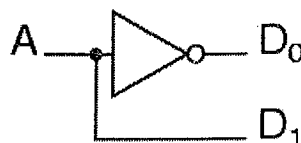


Figure 1

i. Construct a 2-to-4 binary decoder using only 1-to-2 binary decoders and AND gates.

(6 mark)

- ii. A decoder can also have less than 2^n outputs such as the BCD (Binary Coded Decimal) to seven-segment decoder which has 4 inputs and only 7 active outputs to drive a display rather than 16 (2^4) outputs (Figure 2). Propose a circuit that has two (2) seven segment display (SSD)s with a shared decoder to display numbers between zero (0) and ninety nine (99).
 (Hint: Only one (1) SSD will be enabled at a particular time instance. For example, in order to display number 85, first the left most SSD is enabled and 8 is displayed. Then the right most SSD is enabled to display 5.)

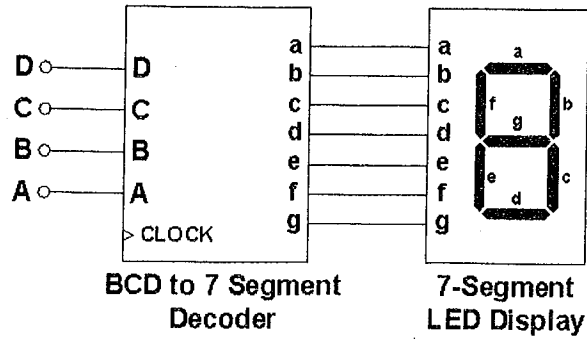


Figure 2

(8 mark)

