Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
300 level 2nd Semester Examination – Dec.-2017/Jan.- 2018
CST353-2 Computer Systems Architecture

Uva Wellassa University

Instructions to candidates
Duration: Two (02) hours
Number of questions: Five (05)
Answer any four (04) questions
Mark allocation: 100

1.

a. Convert the following numbers to equivalent binary numbers.
i. 27_8 ii. 137.25_{10} (4 mark)

b. Represent 1034_{10} as a Binary Coded Decimal value. (2 mark)

c. Convert the following numbers to equivalent decimal numbers.
i. 10110101_2 ii. 11011_8 (4 mark)

d. What is the decimal value of the hexadecimal number 'A0'? (2 mark)

e. In a particular digital device, integers are represented in 8-bits two's complement form. However, the results of computations are display in decimal.
i. Give the representation of $(-13)_{10}$ in the above device. (3 mark)

ii. Explain how the computation of $28_{10} - 13_{10}$ done by the device. All the steps that you have used should be shown in the answer. (6 mark)

f. With the aid of a suitable example in arithmetic addition of binary number system, briefly explain the situation of "overflow". (4 mark)

2.

a. Name and describe the MIPS fields of all instruction types. (3 mark)

b. List and describe the three (03) different types of instruction formats available in MIPS. (6 mark)

c. What are the decimal and binary representations of **add $t0,$s1,$s2** in MIPS fields? (6 mark)

d. Briefly explain the memory hierarchie of a computer using a suitable diagram. (3 mark)

e. List four (04) advantages of having memory hierarchie in a computer. (4 mark)

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f. What are characteristics of the main levels of the memory hierarchy? (3 mark)

3.

a. Briefly explain each line of code of the following assembly program.

```
li $t1, 1                    # li is to load immediate
add $t0, $t1, 2
```

(4 mark)

b. Write the output (register number and value should be included) of the following sample assembly code and describe each line.

```
.globl main
.text
.globl main
#Starting point is the main
main:
        li $t2, 25              # li is for Load immediate
        lw $t3, value           #lw for  Load the word
        add $t4, $t2, $t3
        sub $t5, $t2, $t3

        li $v0, 10
        syscall
.data
value:  .word 12
```

(7 mark)

c. Briefly describe the functions of systems calls. (6 mark)

d. Write an assembly program to read two (02) numbers through keyboard, add them together and display the result. (8 mark)

4.

a. Describe the steps of "Pipelining" process in MIPS architecture. (4 mark)

b. Name and describe three (03) different types of pipelined hazards. (8 mark)

c. Following description is given about a hard disk. The advertised average seek time is 4 ms, the transfer rate is 100 MB/sec, and the controller overhead is 0.2 ms. Assume that the disk is idle so that there is no waiting time. The hard disk is rotating at a speed of 15,000 RPM. What is the average time to read/ write a 512-byte sector from/ to hard disk? (3 mark)

d. Calculate the clock rates of processor P3 and P4 on the following dataset.

	L1 Size	L1 Miss Rate	L1 Hit Rate
P3	2 KB	8.0 %	0.66 ns
P4	4 KB	6.0 %	0.90 ns

(5 mark)

e. A Cache is a two-way set associative cache and it has four (04) blocks. Determine the block number for the memory access sequence 0, 2, 4, 8, 10, 12, 14, 16, 0. (5 mark)

5.

a. Explain the two (02) mechanisms, which are available to write data into the cache. (6 mark)

b. Briefly explain the terms "temporal locality" and "spatial locality". (4 mark)

c. If there are 64 blocks in the cache and the block size is 16 bytes. What is the block number for mapping the address 1200? (2 mark)

d. Describe the following page replacement algorithms using tables assuming the page frame size is four (04) and the page fault for the string is 0 1 2 3 0 1 4 0 1 2 3 4.

i. First In First Out (FIFO) (6 mark)

ii. Least Recently Used (LRU) (7 mark)

Annex

Average Disk Access Time = Average Seek Time + Average Rotational Delay + Transfer Time + Controller Overhead.

Total number of bits in a direct-mapped cache = 2^n * (Block size + Tag size + Valid field size)

CPU time = (CPU execution clock cycles + Memory-stall clock cycles) × Clock cycle time

CPU Clock Cycles = Instructions for a Program * Average clock cycles per instruction

CPU Time = Instruction count * CPI * Clock cycle time

CPU Time = (Instruction Count * CPI) / Clock Rate

CPU Execution Time = CPU Clock Cycles for a Program * Clock Cycle Time

CPU Execution Time = CPU Clock Cycles for a Program / Clock Rate

Memory-stall clock cycles = Read-stall cycles + Write-stall cycles

Average Memory Access Time (AMAT) = Hit time + Miss rate × Miss penalty

Register number 17 = $s1, Register number 18 = $s2 .....

Register number 8 = $t0, Register number 9 = $t1, ...

For addition the opcode value is 0 and the function code value is 32.