Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
200 Level 2nd Semester Examination – Jan. / Feb. 2016
CST 231-2 Microelectronics

Uva Wellassa University

Instructions to candidates:
Duration: Two (02) hours
Number of questions: Four (04)
Answer all questions
Mark allocation: 100
Calculators are **allowed**.

1.

a. Discuss the necessity of converting Analog signals in to Digital.
(3 mark)

b. Explain the meaning of the following terms with respect to signal processing using appropriate examples:
   i. Sampling rate
   ii. Bandwidth
   iii. Bit depth
(6 mark)

c.

i. Using an appropriate example, discuss the impact of sampling rate for the quality of the output of a typical analog to digital conversion.
(3 mark)

ii. The bit-rate of a compressed audio file is specified as 128 kbps while the compression ratio is approximately 10:1. Provided the fact that the sampling rate is 44.1 Khz. Determine the bit-depth (resolution) of the particular audio.
(5 mark)

d.

i. What are the **four (04)** major types of frequency filters?
(4 mark)

ii. Explain the functionality of above (i.) listed frequency filters using frequency response curves.
(4 mark)

2.

a. Briefly explain the process of **doping** in order to manufacture P and N type semiconductors from intrinsic semiconductor materials.
(4 mark)

b. Explain the phenomenon of **diffusion** occurs at any P-N junction prior to formation of the depletion layer.
(4 mark)

c.

i. List **five (05)** Two-terminal semiconductor devices.
(5 mark)

ii. Explain the improved characteristics of any **two (02)** devices selected from the list produced in above (i.) using characteristic curves.
(4 mark)

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d. The forward-bias *i–v* relationship of a typical P-N junction is given below:

$i = I_S(e^{v/V_T} - 1)$ while $V_T = kT/q$

i. Define the terms of the formulae.

(3 mark)

ii. A silicon diode said to be a 1 mA device exhibits a forward voltage of 0.7 V. Given that the values of **k**, V_T and **q** are 8.62 $\times 10^{-5}$ eV/K , 25.3 mV (at room temperature) and 1.60 $\times 10^{-19}$ coulomb, respectively. Evaluate the junction scaling constant (saturation current).

(5 mark)

3.

a. State the conditions should satisfy to switch between the following status of a NPN type Bipolar Junction Transistor.

Hint: Use the terms V_{BE} (Base-Emmitor Voltage), V_{FB} (Forward Bias Voltage), I_B (Base current) and the relationship between I_B, $I_{C,max}$ (The maximum current that will flow across collector) and β (Common Emitter current gain) at each status.

i. Cut-off Region: Transistor acts as an off switch
ii. Active Linear Region: Transistor acts as a current amplifier
iii. Saturation Region: Transistor acts as an on switch
iv. Q-Point (on DC Load-Line)

(8 mark)

b.

i. A bipolar **NPN** transistor has a DC current gain (β) value of 200. Calculate the base current I_B required to switch a resistive load of 6 mA.

(2 mark)

ii. A NPN Transistor has a DC base bias voltage, V_B of 11V and an input base resistor, R_B of 100kΩ. What would be the value of the base current (I_B) into the transistor? Clearly state any assumptions you made.

(3 mark)

c. Consider the following circuit diagram (Figure 01).

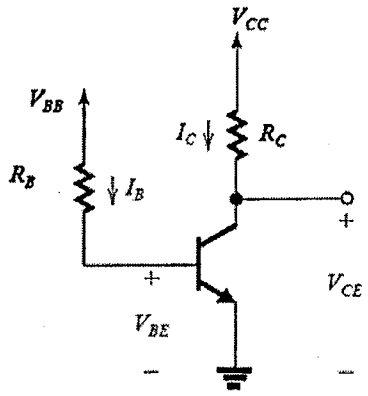

Figure 01: A transistor circuit

For the circuit shown in Figure 01, determine the value of the voltage V_{BB} that results in the transistor operating in following status. Given that V_{cc} = 12 V, R_B = 15 kΩ, R_c = 1.5 kΩ.

(Assume that at the edge of saturation V_{CE} = 0.3 V, V_{BE} remains constant at 0.7 V. The transistor DC current gain β is specified to be 50.)

i. At the active mode with V_{CE} = 5 V

ii. At the edge of saturation

(4 mark)

d. Consider the following schematic diagram of the amplifier circuit (Figure 02).

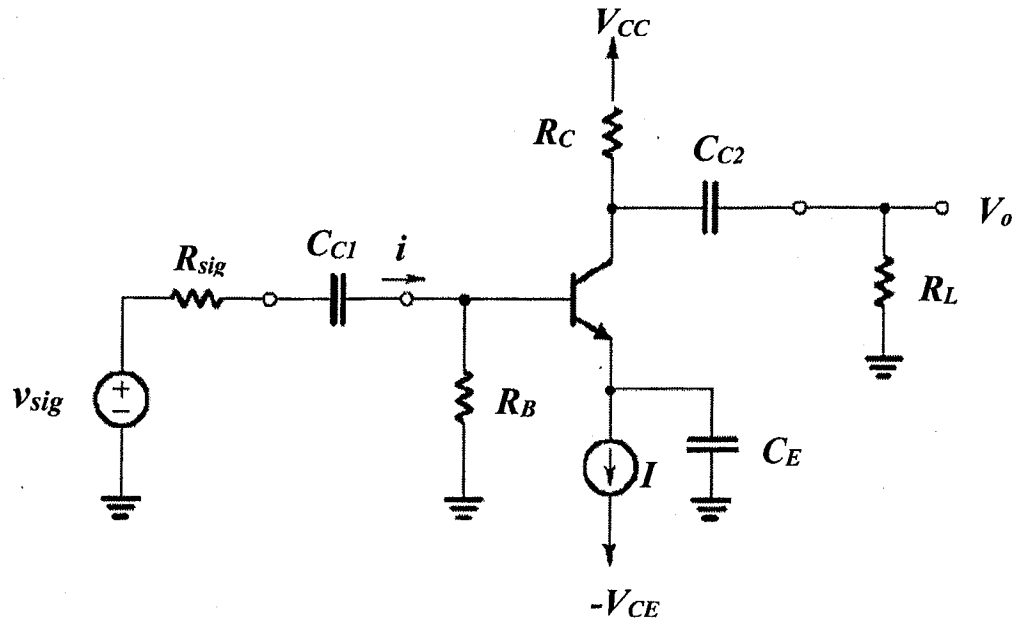

Figure 02: A transistor amplifier circuit

i. Identify the class and the configuration of the amplifier in Figure 02.

(2 mark)

ii. What is the functionality of capacitors C_{C1} and C_{C2}?

(3 mark)

iii. What is the functionality of capacitors C_E?

(3 mark)

4.

a. What are the key advangates of **FETs (Field-Effect Transistors)** compared to **BJT (Bipolar Junction Transistors)**?

(3 mark)

b. Compare and contrast **JFET (Junction Field-Effect Transistor)** against **MOSFET (Metal-Oxide-Semiconductor FET)**.

(4 mark)

c. The Drain current I_D of a **N-Type JFET** for any given bias point in the saturation or active region can be calculated using

$$I_D = I_{DSS} \left[1 - (V_{GS} / V_{GS(cut\text{-}off)}) \right]^2$$

i. Define the terms of the formula.

(3 mark)

ii. If a JFET has a drain current of 9 mA when I_{DSS} = 3 mA and $V_{GS(cut\text{-}off)}$ = – 6 V, find the value of V_{GS}.

(4 mark)

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d.

i. Define the parameters associated with an operational amplifier and specify their ideal values.

(4 mark)

ii. Using appropriate circuit diagrams, explain how to construct an op-amp comparator to compare an analog voltage V with a fixed reference value V_{REF}.

(4 mark)

iii. Explain what is meant by **Hysteresis** using an appropriate example.

(3 mark)