Uva Wellassa University, Sri Lanka
End Semester Examination – March 2011
SCT 361-2 Digital and Analog Electronics

Time: Two (02) hours

Total **06** Questions
Answer **02** questions from **Part-A** and **02** from **Part-B**

PART - A

1) a. What are product terms and sum terms of combinational circuit?

b. i. Convert $Y = \mathrm{ABCD} + \mathrm{A'BC} + \mathrm{B'C'}$ into a sum of minterms by algebraic method.
ii. Convert $\mathrm{Y} = \mathrm{AB} + \mathrm{B'CD}$ into a product of maxterms by algebraic method.

c. Design a logic circuit with four inputs A, B, C and D where the output is to be high only when majority of the inputs are high. Draw the final circuit using only NOR gates.

d. By using Karnough map simplification, derive the logic equations for a circuit that will add two 2-bit binary numbers, $(A_1\, A_0)_2 + (B_1\, B_0)_2$, and produce the sum bits $(S_1\, S_0)_2$ and the carry output bit C_1, as shown below.

$$\begin{array}{r} A_1\; A_0 \\ +\;\; B_1\; B_0 \\ \hline C_1\;\; S_1\; S_0 \end{array}$$

(25 marks)

2) a. What is a multiplexer? Draw the circuit diagram, truth table and give the Boolean equation describing the output, of a 4-to-1 multiplexer.

b. What is the difference between a decoder and a demultiplexer?

c. What is a full-adder? Implement a full-adder circuit using NOR gates only.

d. Use two-input XOR gates to produce the parity generation and checking system that ensures the 4-bit data sent over a serial link is transmitted and received as an odd parity word.

e. An 8-to-1 MUX has inputs A, B and C connected to selection lines S_2, S_1 and S_0 respectively. The data inputs I_0 to I_7 are connected as,

$$I_1 = I_2 = I_7 = 0,\;\; I_3 = I_5 = 1,\;\; I_0 = I_4 = D \text{ and } \;\; I_6 = \overline{D}$$

Determine the Boolean expression of the MUX output.

(25 marks)

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3) a. What is the difference between a latch and a flip-flop?

b. Determine how the circuit shown in Fig. 1 functions as a JK-type flip-flop. Under what input conditions a problem may occur?

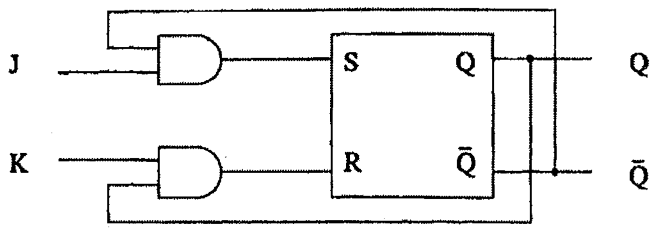

Fig. 1

c. Fig. 2 shows a master-slave flip-flop in which the C input is a square-wave clock signal. Analyze its operation.

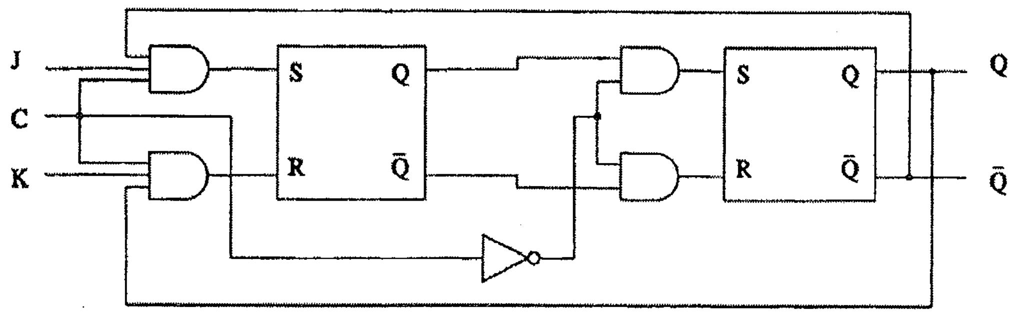

Fig. 2

d. Explain the operation of 4-bit bidirectional shift register with the help of a neat diagram.

e. Design a 4-bit binary ripple counter using negative edge-triggered J-K flip-flops and draw the timing diagram.

(25 marks)

PART - B

4) a. Explain how an OPAMP can be used as a comparator.

b. Draw basic schematic diagrams of both inverting and non-inverting amplifiers.

c. Derive expressions for closed loop gain (G) of both inverting and non-inverting amplifiers.

d. Identify the circuit given in Fig. 3. Derive an equation for its output in terms of inputs and component values. Describe functionality and practical applications.

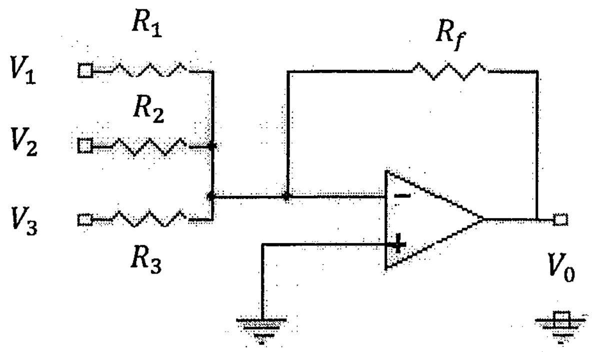

Fig.3

e. Explain the basic integrator circuit using ideal OPAMPs.

(25 marks)

5) a. By using two diodes and relevant components draw voltage doubler circuit. Explain its function.

b. The 6.8V Zener diode in the circuit of Fig.4 is specified to have $V_Z = 6.8V$ at $I_Z = 5mA$. The Zener diode can be replaced with its equivalent circuit model shown in Fig.5, where $r_Z = 20\Omega$. The supply voltage $V^+$is nominally $10V$ but can vary by $\pm 1V$.

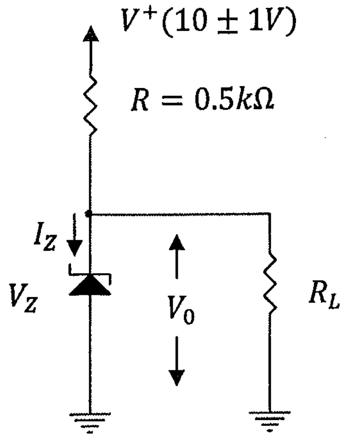

Fig.4

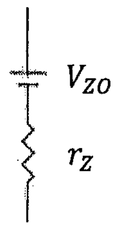

Fig.5

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i. Find V_{Z0} of equivalent circuit model.
ii. Find V_0 with no load and with V^+ at its nominal value.
iii. Find the change in V_0 resulting from the $\pm 1V$ change in V^+.
iv. Find the change in V_0 resulting from connecting a load resistance R_L that draws a current $I_L = 1mA$.
v. Find the change in V_0 when $R_L = 2k\Omega$.
vi. Find the change in V_0 when $R_L = 0.5k\Omega$.
vii. What is the minimum value of R_L for which the diode still operates in the breakdown region? Where knee current, $I_{ZK} = 0.2mA$.

(25 marks)

6) a. What is a Darlington pair? Draw a Darlington pair circuit and derive an expression for current gain (β).

b. Obtain expressions for I_{C2} and I_{B1} for the circuit in Fig.6. Discuss the applications of it.

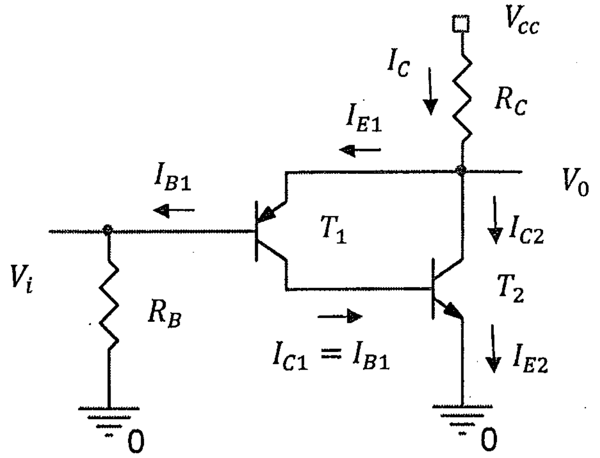

Fig.6

c. Using relevant circuit diagram and characteristic curves explain the BJT's function as a switch.

(25 marks)