Uva Wellassa University, Sri Lanka
End Semester Examination – June 2009

CST 104-2 Microcomputer Architecture & Logic Design

Time: Two (02) hours

Total number of questions 05
Answer **four (04)** questions only

Q1
An industrial robot that places components on a printed circuit board has 3 failsafe sensors and an emergency shutdown switch. The robot should keep functioning unless any of the following conditions arise:

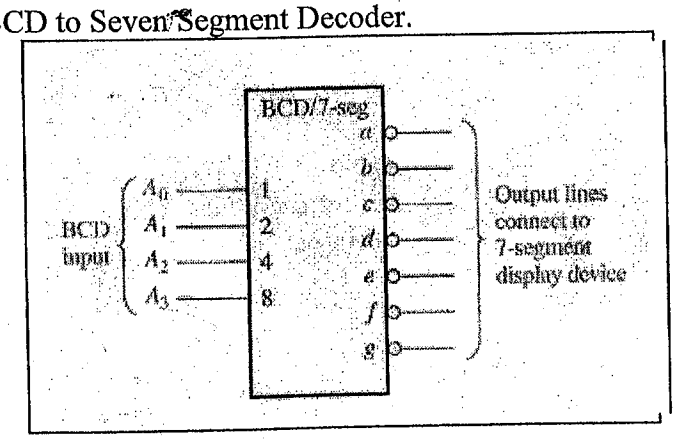
1.) If the emergency switch is pressed the system shuts down.
2.) If sensor 1 and sensor 2 are activated at the same time the system shuts down.
3.) If sensor 2 and sensor 3 are activated at the same time the system shuts down.
4.) If all three sensors are activated at the same time then the system shuts down.

I. Derive the truth table for this system. (Consider functioning of robot as logic 1) **(05 Marks)**

II. Design, using Karnaugh Map techniques, a minimum AND-OR (SOP) gate network for this system. **(10 Marks)**

III. How can an N-input (arbitrary number of inputs) AND gate be constructed from 2-Input AND gates alone? **(10 Marks)**

Q2
Consider the following BCD to Seven Segment Decoder.



I. Draw a table where $A_3A_2A_1A_0$ representing the numbers 0 to 9 in decimal and corresponding outputs of 'a' to 'g'. (10 Marks)

II. Write down the Boolean expression for 'd' in SOP form. (05Marks)
a)Prove above answer. (05Marks)
b)Do the following additions and subtractions using 5 bit 2s complement binary numbers: 8 +4 , 15-7, 5-15 (05Marks)

10

Q3

I. Draw the figures Active High input S-R Latch and Active Low input S-R Latch **(05Marks)**

II. Explain how to operation of Active Low input S-R Latch **(10 Marks)**

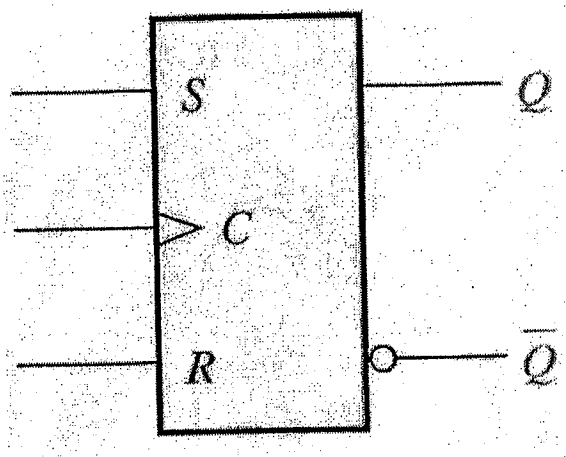
III. Write down the truth table of Active Low input S-R Latch **(05 Marks)**

IV. Draw the waveform according to the about truth table **(05 Marks)**

Q4

I. What is the difference between S-R Flip Flop and J-K Flip Flop? **(05 Marks)**

II.



When ***S*** is High and R is Low the Q output goes High on the triggering edge of the clock pulse. What is the state of this S-R FLIP-FLOP? Draw an Asynchronous counter applying two J-K FLIP FLOPS. **(10 Marks)**

III. If the Flip-Flops operate on +8V DC and draws 5mA of current, what is the power dissipation of that Flip-Flop? Assume that you have a digital system that requires 10 Flip-Flops now what is the total power dissipation? **(10 Marks)**

Q5

I. Write down the equation out put of pulse with of the monostable multivibrater? **(05 Marks)**

II. Assume you have to provide 2.2 KΩ resistor and 0.01 μF capacitor to connect to the monostable multivibrater. Determine the pulse with of the out put pulse? (10 Marks)

III. Draw the complete circuit diagram of monostable multivibrater and explain the operation. (10 Marks)