UVA WELLASSA UNIVERSITY

DEPARTMENT OF COMPUTER SCIENCE & TECHNOLOGY

DEPARTMENT OF SCIENCE & TECHNOLOGY

END SEMESTER EXAMINATION – SEMESTER I – 2007/2008

CST 104-2 MICROCOMPUTER ARCHITECTURE AND LOGIC DESIGN

PHY 231-2 DIGITAL ELECTRONICS AND COMPUTER ARCHITECTURE

Time Allowed: **2 HOURS**

Number of questions: Six (06)
Number of pages: Three (03)

Instructions:

Answer **four (04)** questions **only.**

Clearly state any assumptions made.

Q1: An engine has 4 fail-safe sensors. The engine should keep **running unless** any of the following conditions arise:

- If sensor 2 is activated.
- If sensor 1 and sensor 3 are activated at the same time.
- If sensor 3 and sensor 4 are activated at the same time.

(a) Derive the truth table for this system. [4 marks]

(b) Design, using Karnaugh Map techniques, a minimum AND-OR gate network for this system. Draw the resulting digital circuit diagram. [8 marks]

(c) Design, a digital circuit that will implement the minimal AND-OR gate network found in (b) using both (i) NAND gates only and (ii) NOR gates only. Assume that each logic gate can have any number of inputs and that inverted inputs are available. [6 marks]

(d) If the time delay experienced by a NAND gate is 8ns and the time delay experienced in a NOR gate is 12ns. Which implementation of (c) is faster? By how long? [3 marks]

(e) Prove the rule of Boolean algebra: A+ AB = A+ B [4 marks]

Q2: (a) Explain the operation of a half-adder. What are the logic equations? Draw the logic diagram for a half-adder. [13 marks]

(b) Describe the operation of a full-adder. How is a full adder constructed from two half-adders? In what situation would a half-adder not be sufficient, meaning that a full-adder would be required? [12 marks]

Q3:

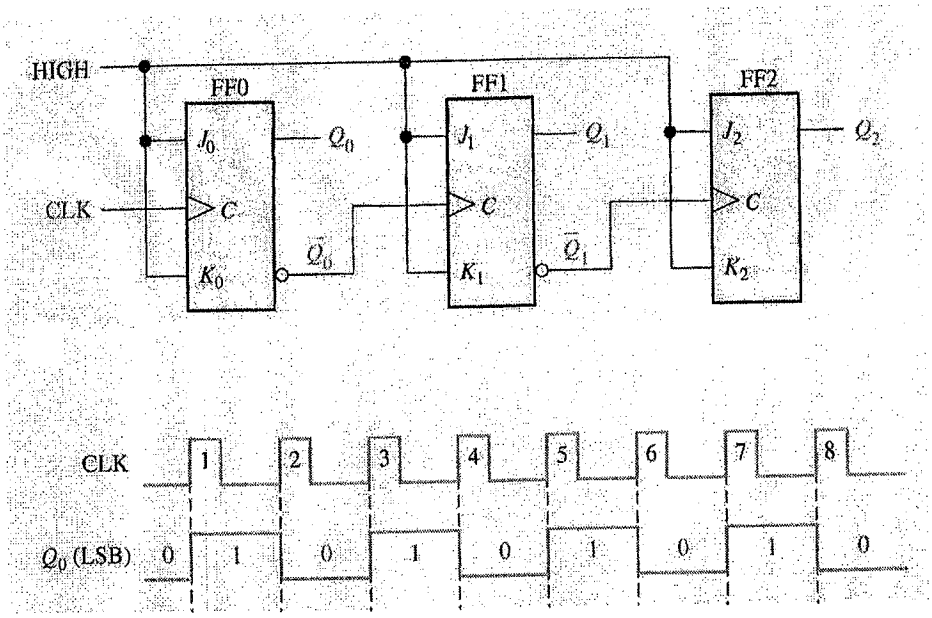
(a) Explain the operation of an exclusive OR gate. Draw the symbol. Calculate the truth table for its operation. [4 marks]

(b) Give 2 ways of expressing an exclusive OR gate using AND, OR and NOT gates. Draw the two expressions as circuits that are equivalent for implementing this operation using AND, OR and NOT gates. [8 marks]

(c) Convert the following decimal number into binary(each step should be shown clearly):
15.758 [6 marks]

(d) Perform the following operation using 6-bit 2's complement binary:
44 – 57 [7 marks]

Q4:



(a) Identify the function of the circuit in above figure. [4 marks]

(b) Complete the timing diagram for Q_1 and Q_2 (MSB) [9 marks]

(c) You are given three negative-edge triggered J-K flip-flops. Using these flip-flops design a circuit to achieve the same functionality as the circuit given above. [8 marks]

(d) If we give a clock pulse with a frequency of 1024Hz to the CLK input in circuit Fig-Q4 what's the frequency of the Q_2 output. [4 marks]

Q5:

(a) Explain the operation of a JK flip-flop (Draw the operation table/truth table). How does it differ from an RS flip-flop? [10 marks]

(b) How can a D flip-flop be used as a 1-bit memory storage device? Use this configuration to build a 4-bit parallel data storage device. You have to draw a circuit diagram including switches to give input and LEDs showing output. [15 marks]

Q6:

(a) Write down 3 digital integrated circuit logic families you know. [3 marks]

(b) What are the most common digital logic families at present? [2 marks]

(c) What's the primary difference between a combinational logic circuit and a sequential logic circuit? [5 marks]

(d) Describe the functionality of following combinational and sequential logic circuits. Include one practical usage of each circuit

i. Decoder ii. Multiplexer iii. Shift Register [15 marks]

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