Uva Wellassa University of Sri Lanka
Faculty of Science and Technology
Department of Computer Science and Technology
300 level 1st Semester Examination – Jul./Aug. 2016
CST331-2 Computer Systems Architecture

Uva Wellassa University

Instructions to candidates
Duration: Two (02) hours
Number of questions: Four (04)
Answer all questions
Mark allocation: 100

01

a. Explain the five (05) addressing modes of MIPS architecture? (5 mark)

b. The following high-level code converts a ten-entry array of characters from lower-case to upper-case by subtracting 32 from each entry.
Translate it into MIPS assembly language.
Hints: The address difference between the array elements is 1 byte. Assume that $s0 already holds the base address of **chararray**.

```
char chararray[10];
int i;
for (i=0; i != 10 ; i=i+1)
        chararray[i] = chararray[i] – 32;
```

(10 mark)

c. Explain the following MIPS code using comments for each line and write one sentence to explain the whole process of the given MIPS code.

```
        add $t0, $zero, $zero
loop:   beq $a1, $zero, finish
        add $t0, $t0, $a0
        sub $a1, $a1, 1
        j loop
finish: addi $t0, $t0, 100
        add $v0, $t0, $zero
```

(6 mark)

d. Explain purposes of the jump and link instruction (jal) and jump register instruction (jr). (4 mark)

(6) (35)

02

a. Describe main four (04) state elements of the MIPS processor. (8 mark)
b. Depict single cycle processor for **sw** and **lw** instructions of the MIPS architecture with appropriate labels. (8 mark)
c. Explain five (05) stages of the pipelined processor. (5 mark)
d. Discuss the statement "Sometimes, there is no way to solve data hazard with forwarding. The alternative solution is stall the pipeline". (4 mark)

03

a. Differentiate temporal and spatial locality. (4 mark)
b. Explain direct mapped cache, N-way set associative cache and full associative cache. (6 mark)
c. Why modern caches are usually write-back instead of write-through write policy? (3 mark)
d. What is the purpose of having a Translation Lookaside Buffer (TLB) in memory systems? (4 mark)
e. Depict the address translation process of virtual memory to physical memory in MIPS architecture (32bit addresses).
Assume that virtual memory size is 2GB (2^{31}bytes), physical memory size is 128MB (2^{27}bytes) and the page size is 4KB (2^{12}bytes). (8 mark)

04

a. Define the following terms.
   i. Multiprocessor
   ii. Cluster
   iii. Parallel processing program
   (3 mark)
b. Explain the two (02) level of hardware schedulers located in Graphic Processing Unit (GPU). (4 mark)
c. Illustrate the block diagram of the multithreaded SIMD processor of a Fermi GPU. (10 mark)
d. The following is a C code for the DAXPY loop. Convert it into CUDA version by assuming that thread block size is 256. (Hint: kernel code and launching the kernel from host parts are adequate). (8 mark)

```
// Invoke DAXPY
Daxpy (n, 2.0, x, y);
//DAXPY in C
Void daxpy (int n, double a, double *x, double *y){
        For (int i=0; i< n; ++i)
                Y[i] = a*x[i] + y[i];
}
```